Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1) (currently amended) A phase locked loop circuit, comprising:

a first circuit ~~capable of providing~~ to provide a current representing frequency; and,

a second circuit, coupled to the first circuit, ~~capable of providing~~ to provide a bias current ~~responsive~~ in response to the current.

2) (original) The circuit of claim 1, wherein the current is obtained from a voltage regulator.

3) (currently amended) The circuit of claim 1, wherein the bias current is provided to a third circuit selected from the group consisting of a charge pump, ~~a~~ loop resistor, phase mixer, amplifier, clock buffer and an equivalent.

4) (currently amended) A delay locked loop circuit, comprising:

a first circuit ~~capable of providing~~ to provide a current representing a delay; and,

a second circuit, coupled to the first circuit, ~~capable of providing~~ to provide a bias current responsive to the current.

5) (original) The circuit of claim 4, wherein the current is obtained from a voltage regulator.

6) (original) The circuit of claim 5, wherein the bias current is provided to a third circuit selected from the group consisting of a charge pump, phase mixer, amplifier, clock buffer and an equivalent.

7) (currently amended) A phase locked loop circuit, comprising:

a phase-frequency detector ~~capable of providing~~ to provide a phase difference signal ~~responsive~~ in response to an input signal and a feedback signal;

a first charge-pump, coupled to the phase-frequency detector, ~~capable of providing~~ to provide a first voltage ~~responsive~~ in response to the phase difference signal;

a second charge pump, coupled to the phase-frequency detector, ~~capable of providing~~

to provide a second voltage ~~responsive~~ in response to the phase difference signal;

a loop resistor, coupled to the first charge-pump, ~~capable of providing~~ to provide a buffered voltage responsive to the first voltage,

a voltage regulator, coupled to the loop resistor and the second charge pump~~, capable of providing~~ to provide a current ~~responsive~~ in response to the buffered voltage and second voltage, wherein the voltage regulator includes a bias-generating device ~~capable of providing~~ to provide a bias current;

a voltage-controlled oscillator, coupled to the voltage regulator, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the current; and,

an interconnect, coupled to the voltage regulator, the first charge pump, and the second charge pump, ~~capable of providing~~ to transfer the bias current.

8) (original) The phase locked loop circuit of claim 7, wherein the bias-generating device in the voltage regulator is a MOSFET device.

9) (currently amended) The phase locked loop circuit of claim 8, wherein the MOSFET device is a first p-type transistor having a drain coupled to the interconnect and the first p-type transistor having a source coupled a voltage source.

10) (currently amended) The phase locked loop circuit of claim 9, wherein the voltage regulator includes:

a second p-type transistor having a gate coupled to a gate of the first p-type transistor and the second p-type transistor having a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the ~~second transistor~~ gate of the second p-type transistor and the third p-type transistor having a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the ~~third transistor~~ gate of the third p-type transistor and the fourth p-type transistor having a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the ~~fourth transistor~~ gate of the fourth p-type transistor and the fifth p-type transistor having a source coupled to the voltage

source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, the first n-type transistor having a source coupled to ground and the first n-type transistor having a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, the drain of the second n-type transistor coupled to the gate ~~and the respective gates~~ of the third p-type transistor and the gate of the fourth p-type transistor ~~transistors~~, the second n-type transistor having a gate coupled to an input, and the second n-type transistor having a source;

a third n-type transistor having a drain coupled to ~~respective drains~~ a drain of the fourth p-type transistor and a drain of the fifth p-type transistor ~~transistors~~, the third n-type transistor having a gate coupled to an output and the gate of the third n-type transistor coupled to the drain ~~respective drains~~ of the fourth p-type transistor and the drain of the fifth ~~transistors~~ p-type transistor, and the third n-type transistor having a source; and,

a fourth n-type transistor having a drain coupled to ~~respective sources~~ the source of the second n-type transistor and the source of the third n-type transistor ~~transistors~~, the fourth n-type transistor having a source coupled to ground and the fourth n-type transistor having a gate coupled to the gate of the first n-type transistor and the drain of the first n-type transistor.

11) (currently amended) A delay locked loop circuit, comprising:

a phase detector ~~capable of generating~~ to generate a phase difference signal ~~responsive~~ in response to an input signal and a feedback signal;

a charge-pump, coupled to the phase detector, ~~capable of generating~~ to generate a voltage ~~responsive~~ in response to the phase difference signal;

a voltage regulator, coupled to the charge pump, ~~capable of providing~~ to provide a current ~~responsive~~ in response to the voltage, wherein the voltage regulator includes a bias-generating device ~~capable of providing~~ to provide a bias current;

a voltage-controlled delay line, coupled to the voltage regulator, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the current; and,

an interconnect, coupled to the charge pump and the voltage regulator, ~~capable of providing~~ to transfer the bias current.

12) (original) The delay locked loop circuit of claim 11, wherein the bias-generating device in the voltage regulator is a MOSFET device.

13) (currently amended) The delay locked loop circuit of claim 12, wherein the MOSFET device is a first p-type transistor having a drain coupled to the interconnect and the first p-type transistor having a source coupled to a voltage source.

14) (currently amended) The delay locked loop circuit of claim 13, wherein the voltage regulator includes:

a second p-type transistor having a gate coupled to a gate of the first p-type transistor and the second p-type transistor having a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the ~~second transistor~~ gate of the second p-type transistor and the third p-type transistor having a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the ~~third transistor~~ gate of the third p-type transistor and the fourth p-type transistor having a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the ~~fourth transistor~~ gate of the fourth p-type transistor and the fifth p-type transistor having a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, the first n-type transistor having a source coupled to ground and the first n-type transistor having a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, the drain of the second n-type transistor coupled to the gate ~~and the respective gates~~ of the third p-type transistor and the gate of the fourth p-type transistor ~~transistors~~, the second n-type transistor having a gate coupled to an input, and the second n-type transistor having a source;

a third n-type transistor having a drain coupled to ~~respective drains~~ a drain of the fourth p-type transistor and a drain of the fifth p-type transistor ~~transistors~~, the third n-type transistor having a gate coupled to an output and the gate of the third n-type transistor

coupled to the drain ~~respective drains~~ of the fourth p-type transistor and the drain of the fifth ~~transistors~~ p-type transistor, and the third n-type transistor having a source; and,

a fourth n-type transistor having a drain coupled to ~~respective sources~~ the source of the second n-type transistor and the source of the third n-type transistor ~~transistors~~, the fourth n-type transistor having a source coupled to ground and the fourth n-type transistor having a gate coupled to the gate of the first n-type transistor and the drain of the first n-type transistor.

15) (currently amended) A circuit, comprising:

a first circuit ~~capable of providing~~ to provide an output signal ~~responsive~~ in response to a comparison of an input signal and a feedback signal; and,

a second circuit, coupled to the first circuit, ~~capable of providing~~ to provide a bias current to the first circuit ~~responsive~~ in response to the input signal.

16) (currently amended) The circuit of claim 15, wherein the first circuit includes a first circuit component that is biased ~~responsive~~ in response to the bias current.

17) (original) The circuit of claim 15, wherein the first circuit component includes a loop resistor.

18) (original) The circuit of claim 15, wherein the first circuit component includes a charge-pump.

19) (original) The circuit of claim 15, wherein the second circuit includes a bias-generating MOSFET device.

20) (original) The circuit of claim 19, wherein the MOSFET device is a p-type device.

21) (original) The circuit of claim 15, wherein the first circuit is a PLL circuit.

22) (original) The circuit of claim 15, wherein the first circuit is a DLL circuit.

23) (currently amended) The circuit of claim 15, wherein the first circuit includes a voltage-controlled oscillator having an input, and the second circuit ~~is capable of generating~~ to generate the bias current proportional to an input current provided to ~~the~~ an input of the voltage-controlled oscillator ~~input~~.

24) (currently amended) A circuit, comprising:

a first p-type ~~device~~ transistor having a gate, the first p-type transistor having a drain ~~capable of outputting~~ to output a current proportional to an output current and the first p-type transistor having a source coupled to a voltage source;

a second p-type transistor having a gate coupled to the gate of the first p-type transistor and the second p-type transistor having a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the gate of the second p-type transistor and the third p-type transistor having a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the gate of -the third p-type transistor and the fourth p-type transistor having a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the gate of the fourth p-type transistor and ~~a~~ the fifth p-type transistor having a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, the first n-type transistor having a source coupled to ground and the first n-type transistor having a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, the drain of the second n-type transistor coupled to the gate ~~and the respective gates~~ of the third p-type transistor and the gate of the fourth p-type transistor ~~transistors~~, the second n-type transistor having a gate coupled to an input, and the second n-type transistor having a source;

a third n-type transistor having a drain coupled to ~~respective drains~~ a drain of the fourth p-type transistor and a drain of the fifth p-type transistor ~~transistors~~, the third n-type transistor having a gate coupled to an output and the gate of the third n-type transistor coupled to the drain ~~respective drains~~ of the fourth p-type transistor and the drain of the fifth p-type transistor ~~transistors~~, and the third n-type transistor having a source; and,

a fourth n-type transistor having a drain coupled to ~~respective sources~~ the source of the second n-type transistor and the source of the third n-type transistor-, the fourth n-type transistor having a source coupled to ground and the fourth n-type transistor having a gate coupled to a gate of the first n-type transistor.

25) (currently amended) The circuit of claim 24, wherein the circuit is included in an operational amplifier ~~capable of generating~~ to generate a buffered signal at the output ~~responsive~~ in response to a signal at the input.

26) (currently amended) A method, comprising:

obtaining a current from a circuit ~~responsive~~ in response to an input signal;

providing a bias current to a circuit component in the circuit ~~responsive~~ in response to the current; and,

biasing the circuit component ~~responsive~~ in response to the bias current.

27) (original) The method of claim 26, wherein the circuit is a PLL.

28) (original) The method of claim 26, wherein the circuit is a DLL.

29) (original) The method of claim 26, wherein the input signal is a clock reference signal.

30) (original) The method of claim 26, wherein the circuit component is a loop resistor.

31) (original) The method of claim 26, wherein the circuit component is a charge-pump.

32) (original) The method of claim 26, wherein the circuit component is a phase mixer.

33) (original) The method of claim 26, wherein the circuit component is an amplifier.

34) (original) The method of claim 26, wherein the circuit component is a clock buffer.

35) (currently amended) A method, comprising:

obtaining a current representing frequency from a voltage regulator in a phase locked loop circuit; and,

providing a bias current to a circuit component in the phase locked loop circuit ~~responsive~~ in response to the current.

36) (currently amended) A method, comprising:

obtaining a current representing delay from a voltage regulator in a delay locked loop circuit; and,

providing a bias current to a circuit component in the delay locked loop circuit in response ~~responsive~~ to the current.

37) (currently amended) A circuit, comprising:

a first circuit ~~capable of providing~~ to provide an output signal ~~responsive~~ in response to a comparison of an input signal and the output signal, wherein the first circuit includes a circuit component; and,

means, coupled to the first circuit, ~~for providing~~ to provide a bias current to the circuit component ~~responsive~~ in response to the input signal.